Voltage-to-Frequency and Frequency-to-Voltage Converter

ADVFC32

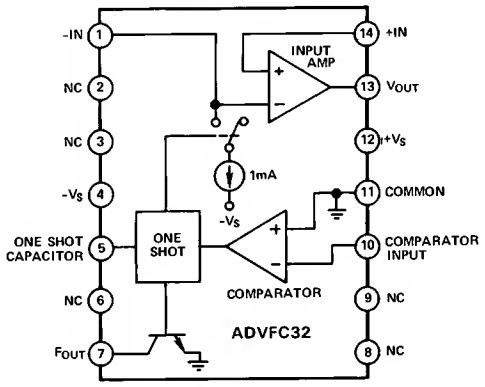
FEATURES

High Linearity
- **±0.01% max at 10 kHz FS**
- **±0.05% max at 100 kHz FS**
- **±0.2% max at 500 kHz FS**

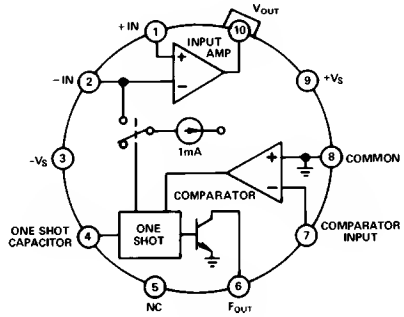
Output TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction
MIL-STD-883 Compliant Versions Available

PIN CONFIGURATION
(TOP VIEW)

"N" Package



"H" Package – TO-100



NC = NO CONNECT

PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage-to-frequency (V/F) converter or frequency-to-voltage (F/V) converter with good linearity (0.01% max error at 10 kHz) and operating frequency up to 0.5 MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using only a few external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15 V or +5 V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8 mA. A larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full-scale calibration drift is held to a maximum of 100 ppm/°C (ADVFC32BH) due to a low T.C. Zener diode.

The ADVFC32 is available in commercial, industrial, and extended temperature grades. The commercial grade is packaged in a 14-pin plastic DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans.

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to high accuracy voltage-to-frequency conversion. The full-scale operating frequency is determined by only one precision resistor and capacitor. The tolerance of other support components (including the integration capacitor) is not critical. Inexpensive ±20% resistors and capacitors can be used without affecting linearity or temperature drift.
2. The ADVFC32 is easily configured to satisfy a wide range of system requirements. Input voltage scaling is set by selecting the input resistor which sets the input current to 0.25 mA at the maximum input voltage.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. The ADVFC32 is intended as a pin-for-pin replacement for VFC32 devices from other manufacturers.
5. The ADVFC32 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current ADVFC32/883B data sheet for detailed specifications.

REV. A

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ADVFC32– SPECIFICATIONS (typical @ +25°C with V_S = ±15 V unless otherwise noted)

Model	ADVFC32K Min	ADVFC32K Typ	ADVFC32K Max	ADVFC32B Min	ADVFC32B Typ	ADVFC32B Max	ADVFC32S Min	ADVFC32S Typ	ADVFC32S Max	Units
DYNAMIC PERFORMANCE										
Full Scale Frequency Range	0		500	0		500	0		500	kHz
Nonlinearity[1]										
f_{MAX} = 10 kHz	–0.01		±0.01	–0.01		+0.01	–0.01		+0.01	%
f_{MAX} = 100 kHz	**–0.05**		**+0.05**	**–0.05**		**+0.05**	**–0.05**		**+0.05**	%
f_{MAX} = 0.5 MHz	–0.20	±0.05	+0.20	–0.20	±0.05	+0.20	–0.20	±0.05	+0.20	%
Full-Scale Calibration Error (Adjustable to Zero)		±5			±5			±5		%
vs. Supply (Full Scale Frequency = 100 kHz)	**–0.015**		**+0.015**	**–0.015**		**+0.015**	**–0.015**		**+0.015**	% of FSR%
vs. Temperature (Full Scale Frequency = 10 kHz)		±75		–100		+100	**+150**		**+150**	ppm/°C
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			
Overload Recovery Time	1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			
ANALOG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range	0		+0.25	0		+0.25	0		+0.25	mA
Voltage Input Range	0		–10 0.25 × R_{IN}[3]	0		–10 0.25 × R_{IN}[3]	0		–10 0.25 × R_{IN}[3]	V^2 mA
Differential Impedance	300 kΩ‖10 pF	2 MΩ‖10 pF		300 kΩ‖10 pF	2 MΩ‖10 pF		300 kΩ‖10 pF	2 MΩ‖10 pF		
Common-Mode Impedance	300 MΩ‖3 pF	750 MΩ‖3 pF		300 MΩ‖3 pF	750 MΩ‖10 pF		300 MΩ‖3 pF	750 MΩ‖10 pF		
Input Bias Current										
Noninverting Input		40	**250**		40	**250**		40	**250**	nA
Inverting Input	**–100**	±8	**+100**	**–100**	±8	**+100**	**–100**	±8	**+100**	nA
Input Offset Voltage (Trimmable to Zero)[2, 3]			**4**			**4**			**4**	mV
vs. Temperature (T_{MIN} to T_{MAX})			30			30			**30**	µV/°C
Safe Input Voltage		±V_S			±V_S			±V_S		
COMPARATOR (F/V Conversion)										
Logic "0" Level	–V_S		–0.6	–V_S		–0.6	–V_S		–0.6	V
Logic "1" Level	+1		+V_S	+1		+V_S	+1		+V_S	V
Pulse Width Range[4]	0.1		0.15/f_{MAX}	0.1		0.15/f_{MAX}	0.1		0.15/f_{MAX}	µs
Input Impedance	50 kΩ‖10 pF	250 kΩ		50 kΩ‖10 pF	250 kΩ		50 kΩ‖10 pF	250 kΩ		
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0" I_{SINK} = 8 mA			**0.4**			**0.4**			**0.4**	V
Output Leakage Current in Logic "1"			**1**			**1**			**1**	µA
Voltage Range	0		+30	0		+30	0		+30	V
Fall Times (Load = 500 pF and I_{SINK} = 5 mA)			400			400			400	ns
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (0 mA≤I_O≤7 mA)	0		+10	0		+10	0		+10	V
Source Current (0≤V_O≤7 V)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
Closed Loop Output Impedance			1			1			1	Ω
POWER SUPPLY										
Rated Voltage		±15			±15			±15		V
Voltage Range	±9		±18	±9		±18	±9		±18	V
Quiescent Current		6	**8**		6	**8**		6	**8**	mA
TEMPERATURE RANGE										
Specified Range	0		+70	–25		+85	–55		+125	°C
Operating Range	–25		+85	–55		+125	–55		+125	°C
Storage	–25		+85	–65		+150	–65		+150	°C
PACKAGE OPTIONS										
Plastic DIP (N-14)		ADVFC32KN								
TO–100 (H-10A)					ADVFC32BH			ADVFC32SH		

NOTES
[1]Nonlinearity defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.
[2]See Figure 3.
[3]See Figure 1.
[4]f_{MAX} expressed in units of MHz.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

UNIPOLAR V/F, POSITIVE INPUT VOLTAGE

When operated as a V/F converter, the transformation from voltage to frequency is based on a comparison of input signal magnitude to the 1 mA internal current source.

A more complete understanding of the ADVFC32 requires a close examination of the internal circuitry of this part. Consider the operation of the ADVFC32 when connected as shown in Figure 1. At the start of a cycle, a current proportional to the

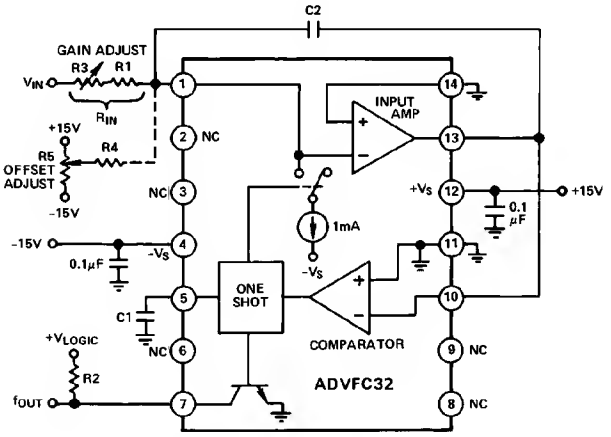


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

input voltage flows through R3 and R1 to charge integration capacitor C2. As charge builds up on C2, the output voltage of the input amplifier decreases. When the amplifier output voltage (Pin 13) crosses ground (see Figure 2 at time t_1), the comparator triggers a one shot whose time period is determined

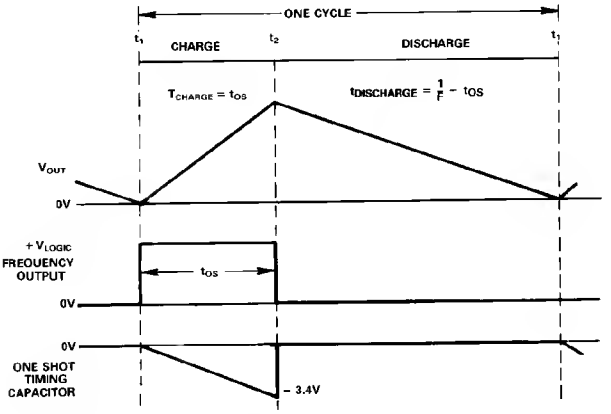


Figure 2. Voltage-to-Frequency Conversion Waveforms

by capacitor C1. Specifically, the one shot time period (in nanoseconds) is:

$$t_{OS} \cong (C_1 + 44\ pF) \times 6.7\ k\Omega$$

During this period, a current of (1 mA – I_{IN}) flows out of the integration capacitor. The total amount of charge depleted during one cycle is, therefore (1 mA – I_{IN}) × t_{OS}. This charge is replaced during the remainder of the cycle to return the integrator to its original voltage. Since the charge taken out of C2 is equal to the charge that is put on C2 every cycle,

$$(1\ mA - I_{IN}) \times t_{OS} = I_{IN} \times \left(\frac{1}{F_{OUT}} - t_{OS}\right)$$

or, rearranging terms,

$$F_{OUT} = \frac{I_{IN}}{1mA \times t_{OS}}$$

The complete transfer equation can now be derived by substituting $I_{IN} = V_{IN}/R_{IN}$ and the equation relating C1 and t_{OS}. The final equation describing ADVFC32 operation is:

$$\frac{V_{IN}\ /\ R_{IN}}{1mA \times (C_1 + 44\ pF) \times 6.7k\Omega}$$

Components should be selected to optimize performance over the desired input voltage and output frequency range using the equations listed below:

$$\frac{3.7 \times 10^7\ pF\ /sec}{F_{OUT\ FS}} - 44\ pF$$

$$C_2 = \frac{10^{-4}\ Farads/sec}{F_{OUT\ FS}} (1000\ pF\ \ minimum)$$

$$R_{IN} = \frac{V_{IN\ FS}}{0.25\ mA}$$

$$R_2 \geq \frac{+V_{LOGIC}}{8\ mA}$$

Both R_{IN} and C_1 should have very low temperature coefficients as changes in their values will result in a proportionate change in the V/F transfer function. Other component values and temperature coefficients are not critical.

Table I. Suggested Values for C_1, R_{IN} and C_2

$V_{IN\ FS}$	$F_{OUT\ FS}$	C_1	R_{IN}	C_2
1 V	10 kHz	3650 pF	4.0 kΩ	0.01 μF
10 V	10 kHz	3650 pF	40 kΩ	0.01 μF
1 V	100 kHz	330 pF	4.0 kΩ	1000 pF
10 V	100 kHz	330 pF	40 kΩ	1000 pF

ORDERING GUIDE

Part Number[1]	Gain Tempco ppm/°C	Temp Range °C	Package Option
ADVFC32KN	±75 typ	0 to +70	14-Pin Plastic DIP
ADVFC32BH	±100 max	–25 to +85	TO-100
ADVFC32SH	±150 max	–55 to +125	TO-100

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current ADVFC32/883B data sheet.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADVFC32 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Input resistance R_{IN} is composed of a fixed resistor (R1) and a variable resistor (R3) to allow for initial gain error compensation. To cover all possible situations, R3 should be 20% of R_{IN}, and R1 should be 90% of R_{IN}. This allows a ±10% gain adjustment to compensate for the ADVFC32 full-scale error and the tolerance of C1.

If more accurate initial offset is required, the circuit of R4 and R5 can be added. R5 can have a value between 10 kΩ and 100 kΩ, and R4 should be approximately 10 MΩ. The amount of current required to trim zero offset will be relatively small, so the temperature coefficients of these resistors are not critical. If large offsets are added using this circuit, temperature drift of both of these resistors is much more important.

BIPOLAR V/F

By adding another resistor from Pin 1 (Pin 2 of TO-100 can) to a stable positive voltage, the ADVFC32 can be operated with a bipolar input voltage. For example, an 80 kΩ resistor to +10 V causes an additional current of 0.125 mA to flow into the integrator so that the net current flow to the integrator is positive even for negative input voltages. At negative full-scale input voltage, 0.125 mA will flow into the integrator from V_{IN} cancelling out the 0.125 mA from the offset resistor, resulting in an output frequency of zero. At positive full scale, the sum of the two currents will be 0.25 mA and the output will be at its maximum frequency.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 3 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full-scale output frequency occurs at negative full-scale input, and zero output frequency corresponds to zero input voltage.

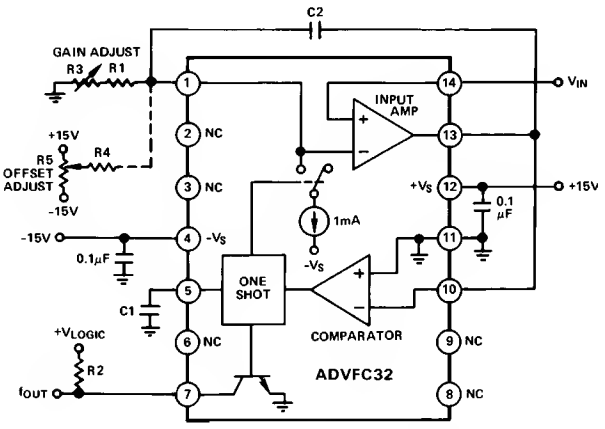


Figure 3. Connection Diagram for V/F Conversion, Negative Input Voltage

A very high impedance signal source may be used since it only drive the noninverting integrator input. Typical input impedance at this terminal is 250 MΩ or higher. For V/F conversion of positive input signals the signal generator must be able to source 0.25 mA to properly drive the ADVFC32, but for negative V/F conversion the 0.25 mA integration current is drawn from ground through R1 and R3.

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in the previous section. For best operating results use component equations listed in that section.

F/V CONVERSION

Although the mathematics of F/V conversion can be very complex, the basic principle is easy to understand. Figure 4 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1 mA into the integrator input for a measured time period (determined by C1). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

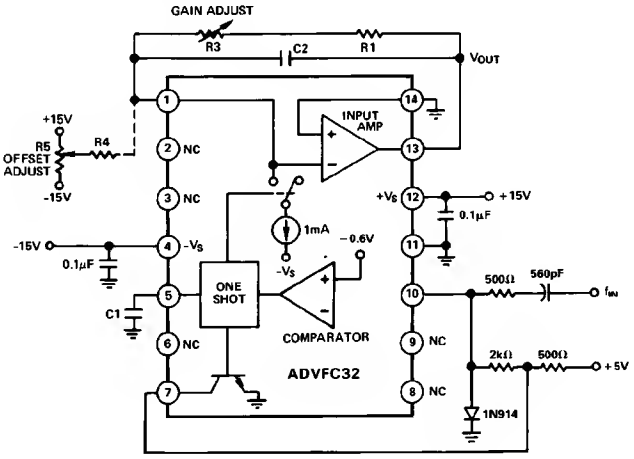


Figure 4. Connection Diagram for F/V Conversion, TTL Input

DECOUPLING

Decoupling power supplies at the device is good practice in any system, but absolutely imperative in high resolution applications. For the ADVFC32, it is important to remember where the voltage transients and ground currents flow. For example, the current drawn through the output pulldown transistor originates from the logic supply, and is directed to ground through Pin 11 (Pin 8 of TO-100). Therefore, the logic supply should be decoupled near the ADVFC32 to provide a low impedance return path for switching transients. Also, if there is a separate digital ground it should be connected to the analog ground at the ADVFC32. This will prevent ground offsets that could be created by directing the full 8 mA output current into the analog ground, and subsequently back to the logic supply.

Although some circuits may operate satisfactorily with the power supplies decoupled at only one location on each board, this practice is not recommended for the ADVFC32. For best results, each supply should be decoupled with 0.1 µF capacitor at the ADVFC32. In addition, a larger board level decoupling capacitor of 1 µF to 10 µF should be located relatively close to the ADVFC32 on each power supply.

COMPONENT TEMPERATURE COEFFICIENTS

The drift specifications of the ADVFC32 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C1 directly affect the overall temperature stability. In the application of Figure 2, a 10 ppm/°C input resistor used with a

100 ppm/°C capacitor may result in a maximum overall circuit gain drift of:

100 ppm/°C (ADVFC32BH) + 100 ppm/°C (C1)
+ 10 ppm/°C (R_{IN}) = 210 ppm/°C

Although R_{IN} and C1 have the most pronounced effect on temperature stability, the offset circuit of resistors R4 and R5 may also have a slight effect on the offset temperature drift of the circuit. The offset will change with variations in the resistance of R4 and supply voltage changes. In most applications the offset adjustment is very small, and the offset drift attributable to this circuit will be negligible. In the bipolar mode, however, both the positive reference and the resistor used to offset the signal range will have a pronounced effect on offset drift. A high quality reference and resistor should be used to minimize offset drift errors.

Other circuit components do not directly influence temperature performance as long as their actual values are not so different from nominal value as to preclude operation. This includes integration capacitor C2. A change in the capacitance value of C2 results in a different rate of voltage change across C2, but this is compensated by an equal effect when C2 is discharged by the switched 1 mA current source so that no net effect occurs.

The temperature effects of the components described above are the same when the ADVFC32 is configured for negative or bipolar input ranges, or F/V conversion.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to Pins 1, 13, and 14 is not a standard operational amplifier. Although it operates like an op amp in most applications, two key differences should be noted. First, the bias current of the positive input is typically 40 nA while the bias current of the inverting input is ±8 nA. Therefore, any attempt to cancel input offset voltage due to bias currents by matching input resistors will create worse offsets. Second, the output of this amplifier will sink only 1 mA, even though it will source as much as 10 mA. When used in the F/V mode, the amplifier must be buffered if large sink currents are required.

MICROPROCESSOR OPERATED A/D CONVERTER

With the addition of a few external components the ADVFC32 can be used as a ±10 V A/D microprocessor front end. Although the nonlinearity of the ADVFC32 is only 0.05% maximum (0.01% typ), the resolution is much higher, allowing it to be used in 16-bit measurement and control systems where a monotonic transfer function is essential. The resolution of the circuit shown in Figure 5 is dependent on the amount of time allowed to count the ADVFC32 frequency output. Using a full scale frequency of 100 kHz, an 8-bit conversion can be made in about 10 ms, and a 2 second time period allows a 16-bit measurement, including offset and gain calibration cycles.

As shown in Figure 5, the input signal is selected via the AD7590 input multiplexer. Positive and negative references as well as a ground input are provided to calibrate the A/D. This is very important in systems subject to moderate or extreme temperature changes since the gain temperature coefficient of the ADVFC32 is as high as ±150 ppm/°C. By using the calibration cycles, the A/D conversion will be as accurate as the references provided. The AD542 following the input multiplexer provides a high impedance input (10^{12} ohms) and buffers the switch resistance from the relatively low impedance ADVFC32 input.

If higher linearity is required, the ADVFC32 can be operated at 10 kHz, but this will require a proportionately longer conversion, time. Conversely, the conversion time can be decreased at the expense of nonlinearity by increasing the maximum frequency to as high as 500 kHz.

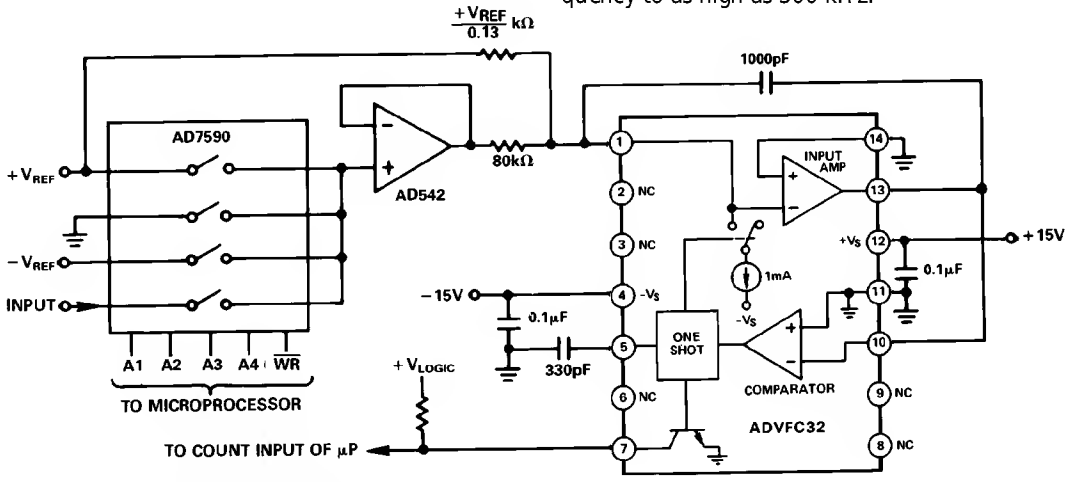


Figure 5. High Resolution, Self-Calibrating, Microprocessor Operated A/D Converter

HIGH NOISE IMMUNITY, HIGH CMRR ANALOG DATA LINK

In many applications, a signal must be sensed at a remote site and sent through a very noisy environment to a central location for further processing. In these cases, even a shielded cable may not protect the signal from noise pickup. The circuit of Figure 6 provides a solution in these cases. Due to the optocoupler and voltage-to-frequency conversion, this data link is extremely insensitive to noise and common-mode voltage interference. For even more protection, an optical fiber link substituted for the HCPL2630 will provide common-mode rejection of more than several hundred kilovolts and virtually total immunity to electrical noise. For most applications, however, the frequency modulated signal has sufficient noise immunity without using an optical

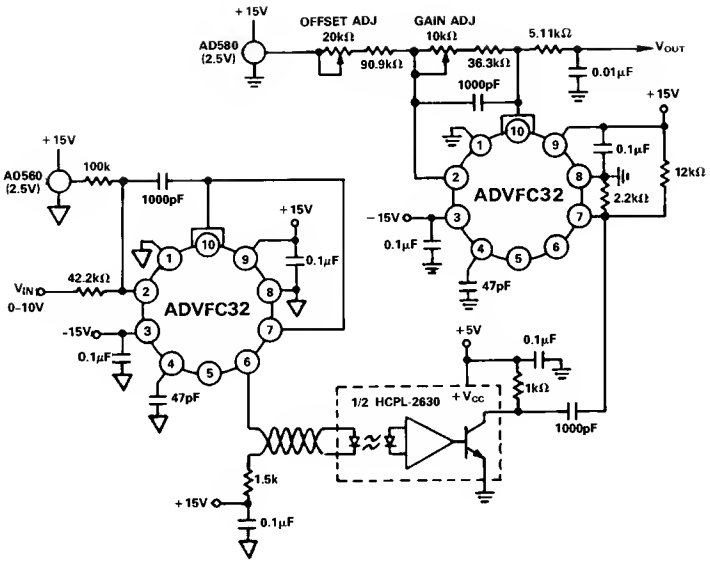


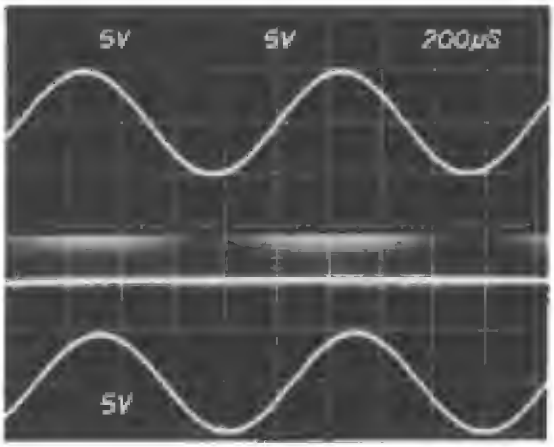
Figure 6. High Noise Immunity Data Link

fiber link, and the optocoupler provides common-mode isolation up to 3000 V dc.

The data link input voltage is changed in a frequency modulated signal by the first ADVFC32. A 42.2 kΩ input resistor and a 100 kΩ offset resistor set the scaling so that a 0 V input signal corresponds to 50 kHz, and a 10 V input results in the maximum output frequency of 500 kHz. A high frequency optocoupler is then used to transmit the signal across any common-mode voltage potentials to the receiving ADVFC32. The optocoupler is not necessary in systems where common-mode noise is either very small or a constant low level dc voltage. In systems where common-mode voltage may present a problem, the connection between the two locations should be through the optocoupler; no power or ground connections need to be made.

The output of the optocoupler drives an ADVFC32 hooked up in the F/V configuration. Since the reconstructed signal at Pin 10 has a considerable amount of carrier feedthrough, it is desirable to filter out any frequencies in the carrier range of 50 kHz to 500 kHz. The frequency response of the F/V converter is only 3 kHz due to the pole made by the integrator, so a second 3 kHz filter will not significantly limit the bandwidth. With the simple one pole filter shown in Figure 6, the input to output 3 dB point is approximately 2 kHz, and the output noise is less than 15 mV. If a lower output impedance drive is needed, a two pole active filter is recommended as an output stage.

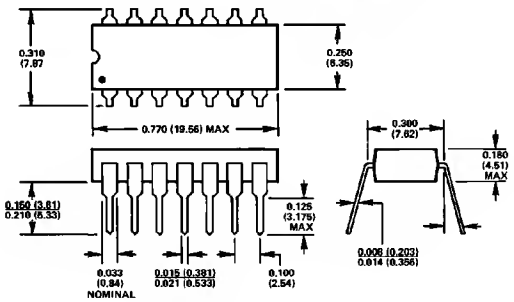
Although the F/V conversion technique used in this circuit is quite simple, it is also very limited in terms of its frequency response and output ripple. The frequency response is limited by the integrator time constant and while it is possible to decrease that time constant, either signal range or output ripple must be sacrificed. The performance of the circuit of Figure 6 is shown in the photograph below. The top trace is the input signal, the middle trace is the frequency-modulated signal at the optocoupler's output, and the bottom trace is the recovered signal at the output of the F/V converter.



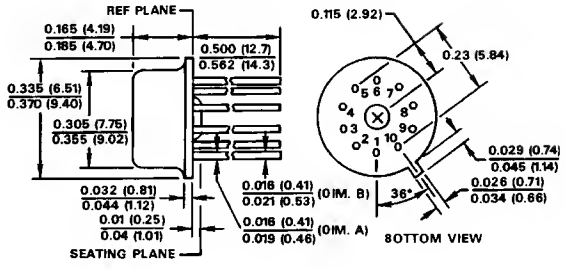
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Pin Plastic DIP Package



TO-100 Package



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